A SNAP-SHOT CMOS ACTIVE PIXEL IMAGER FOR LOW-NOISE, HIGH-SPEED IMAGING

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ABSTRACT

Recent advances in CMOS imager technology have enabled the development of highly integrated, ultra-low power, camera-on-a-chip with impressive imaging performance. However, the most CMOS imagers do not support simultaneous integration of all pixels in the imager. The non-simultaneous exposure leads to image distortion whenever there is relative motion between the imager and the scene. Previous approaches to implementing snap-shot CMOS imagers have required either modification of the standard CMOS process or addition of in-pixel storage elements in a manner that increases noise and decreases optical collection efficiency.

In this paper, we report a new design of an electronically-shuttered, snap-shot CMOS imager implemented in a single-poly standard CMOS process. The imager chip is capable of imaging at high shutter speeds, producing high quality images free from motion artifacts. Design considerations for achieving imaging performance commensurate with that of a state-of-the-art CMOS imager are presented. The imager chip is designed with a goal to achieve high quantum efficiency (QE), good blooming control, low dark current, low noise, and low image lag. The paper reports and discusses test results from a prototype 128x128 snap-shot photogate imager, designed and fabricated in a 0.5 μm standard CMOS technology.

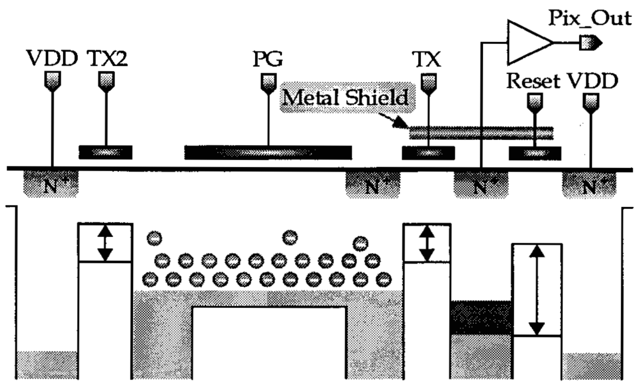
Figure 1a shows the schematic of the pixel of the snap-shot CMOS imager, consisting of a photogate (PG), two transfer gates (TX and TX2), and a reset gate (RESET). The transfer gates are common to the entire chip. As a result of using standard single-poly CMOS technology, the gates are separated by floating n^+ diffusions. Figure 1b shows the layout of a pixel of 14.4 μm pitch, and 27% fill factor. Both TX and TX2 are operated in pulsed mode, with TX2 acting as a lateral overflow gate. Pulsing TX allows simultaneous transfer of charges under PG to the respective sense nodes, enabling snap-shot image capture. The sense node provides a frame buffer, allowing high-speed exposure independent of the read time.

The exposure time is defined by the pulse duration of PG. However, even after PG is turned OFF, the floating diffusions continue to collect photo-charges. Transfer of these unwanted charges into the sense node is responsible for image lag and excess noise. The paper reports a technique for eliminating image lag, by pulsing TX2 and PG in a way that preferentially drains outs unwanted charges through the lateral overflow drain. The paper details the clocking scheme and the relationships between the clock levels necessary for minimizing lag and noise. Given that the snap-shot imaging mode precludes the use of on-chip correlated double sampling technique, it also discusses the pixel design for achieving noise floor below 10 e^-.

Figure 2a is a photograph of the imager chip, and figure 2b shows the image of dollar bill captured with the imager. Test results summarized in table 1 indicate that the imager is capable of achieving high image quality. As expected, the chip draws little power - only 3 mW at 1 Mpix./sec. The measured read noise is less than 10 e^-, and the addition of TX2 and sense node shield has minimal effect (< 10%) on QE. Figure 3 shows that the transfer characteristic exhibits excellent linearity. Linear exposure control is obtained down to 90 μsec.

Figures 4a and 4b depict the images of a fast-rotating fan (1800 r.pm.) captured at video rate and at 100 μsec. exposures respectively. "Freezing" of the fan motion (in figure 4b) demonstrates artifact-free high-speed imaging capability of the chip. Due to a shorter exposure time, light collected by the image in figure 4b is over 100 times less. Experimental results indicate that the image exhibits no blooming, even when the scene was spot-illuminated at levels 80 dB higher than saturation, as shown in figure 5. The dark current rate depends on the exposure time, with the dark signal per pixel varying from 4 to 30 e^- for exposure variations from 100 μsec. to 30 msec. at 500 kHz data readout. Relative contributions of dark current from photogate and sense node are presented in the paper, along with a discussion on stray light coupling into the sense node. Figure 6 shows images from two consecutive frames, a dark frame followed by a bright one. No residual image was observed, and measurements indicate over 74 dB (full dynamic range) image lag suppression.

In conclusion, the imager chip performance demonstrates high quality imaging from an electronically shuttered CMOS imager operating at high shutter speeds and with simultaneous integration. The test results verify that the goal of developing a snap-shot imager that does not compromise image performance and is implemented in a single-poly standard CMOS technology has been achieved.



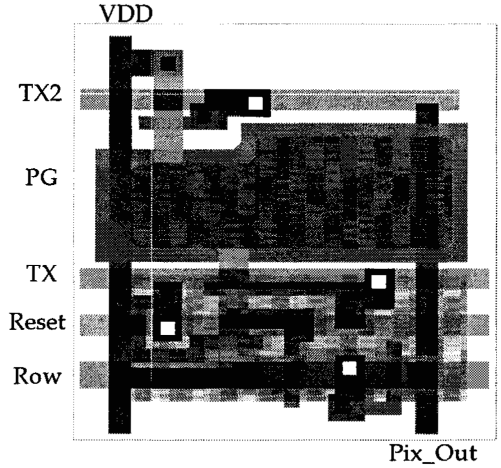
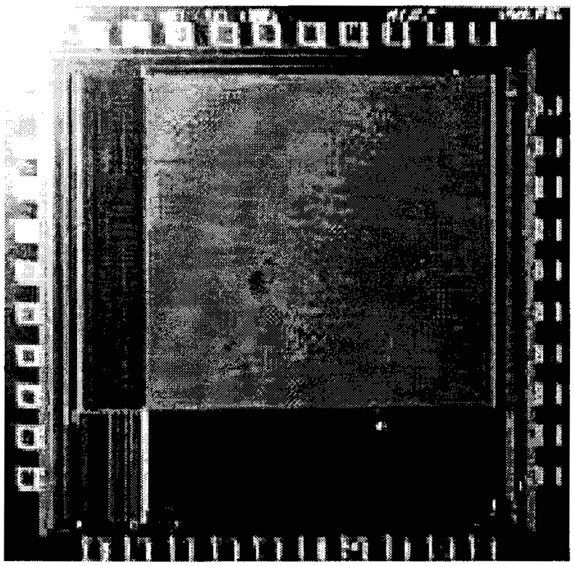


Figure 1a: *Snap-shot imager pixel schematic with potential well diagram;* **Figure 1b**: *Pixel layout*



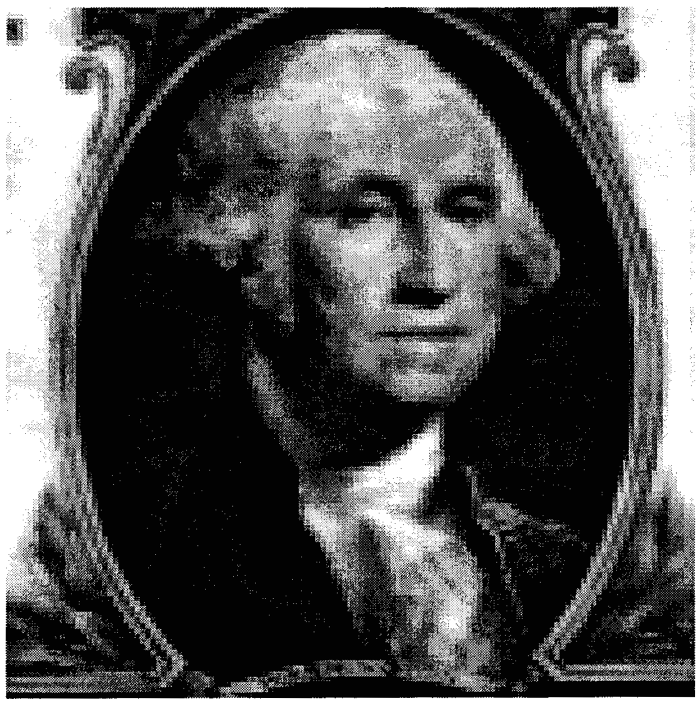


Figure 2a: *Photograph of the imager chip;* **Figure 2b**: *Image of "george" captured at video rate*

Table 1. *Summary of design specifications and present test results of the snapshot APS.*

Array Format	128x128	*Peak QE*	18%
Pixel Type	Photogate	*Linearity*	> 99.9% over 90% of range
Fabrication Process	14.4-μmx14.4-μm	*Read Noise*	< 10 electrons
Pixel Size	HP 0.5-μm ; 3-metal, 1-poly	*Full Well*	> 50,000 electrons
Complexity	6 transistors per pixel	*Dynamic range*	74 dB
Conversion Gain	25 μV/e$^-$	*Min. Exposure Time*	< 90 μsec
Fixed Pattern Noise	0.1% after DDS correction	*Dark Rate*	10 – 77 pA/cm^2 @ R.T.
Max. frame rate	400 frames/sec.	*Image lag*	< 74 dB
Power	< 3 mW @ 1 Mpix./sec	*Blooming control*	> 80 dB above saturation

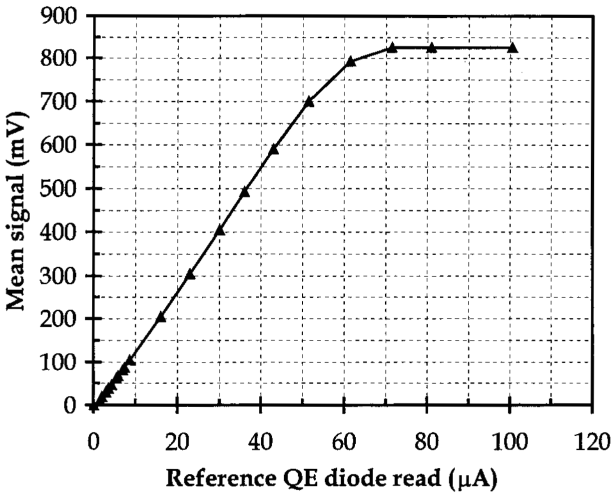


Figure 3: *Imager transfer characteristic*

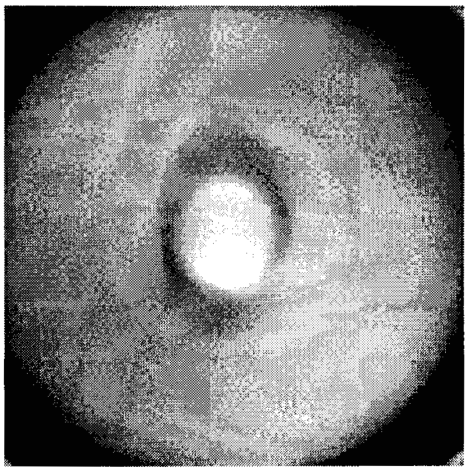


Figure 4a: *Image of a rotating fan at 30 msec. exposure*

Figure 4b: *Image of a rotating fan at 100 μsec. exposure*

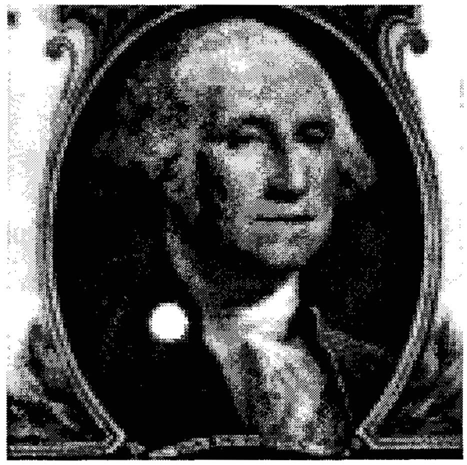


Figure 5: *Image of "George" with laser spot illumination*

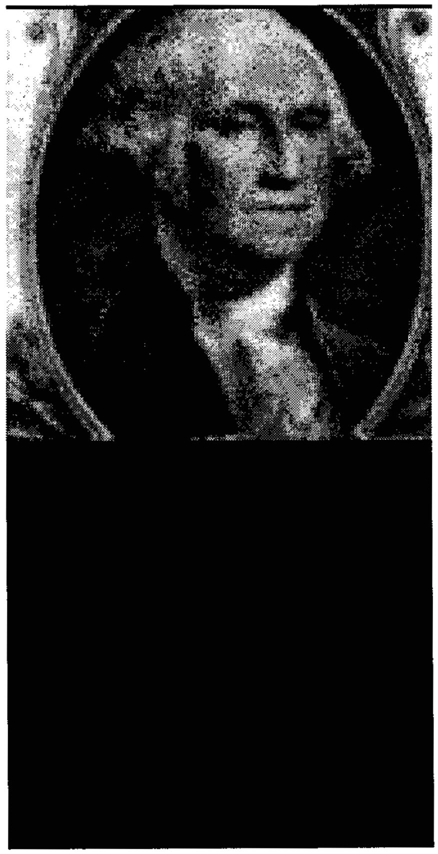


Figure 6: *Image of "George" from consecutive frames with varying illumination levels*